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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/724,750 | 12/02/2003 | Akira Hamamatsu | 520.43302PX1 | 2088 |

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| EXAMINER | |
|---|---|
| STAFIRA, MICHAEL PATRICK | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2877 | |

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/724,750 | HAMAMATSU ET AL. | |
| | Examiner | Art Unit | |
| | Michael P. Stafira | 2877 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *amendment file 1/17/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2 and 4-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

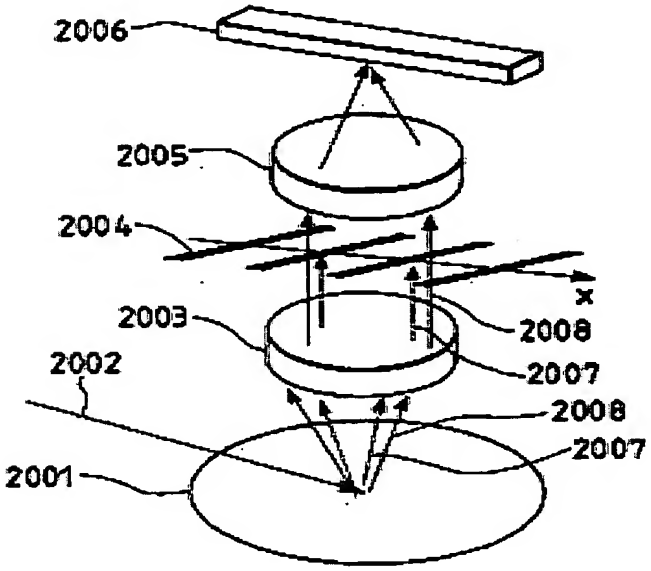
3. Claims 1-2, 4-7are rejected under 35 U.S.C. 102(b) as being anticipated by Morioka et al. ('459).

**Claim 1**

Morioka et al. ('459) discloses illuminating light (Fig. 2, Ref. 2002) to an inspection object containing repetitive circuit patterns formed on a surface (Fig. 2, Ref. 2001); detecting an image (Fig. 2, Ref. 2006) signal corresponding to transmission light by selectively shielding a diffraction light pattern (Fig. 2, Ref. 2004) generated from said repetitive circuit patterns when the illuminating light is reflected from the surface of said inspection object (Col. 9, lines 6-18); and detecting the defects existing on the surface of the inspection object by processing the detected image signal (Col. 9, lines 44-60); wherein said selective shielding of said diffraction light pattern in said detecting step is

performed by a substrate or a film which is etched so as to leave shielding patterns (See Fig. 2).

FIG. 2




**Claim 2**

Maeda et al. ('498) further discloses the repetitive circuit patterns comprise a plurality of chips formed on the surface (Col. 9, lines 39-42) of the inspection object (Fig. 2, Ref. 2001) and said selective shielding (Fig. 2, Ref. 2004) of the diffraction light pattern is performed according to a change of the diffraction light pattern for every area in one chip obtained by detecting diffraction light patterns for one chip as a Fourier transform image (Col. 9, lines 6-18).

**Claim 4**

Morioka et al. ('459) discloses an illumination optical system (Fig. 2, Ref. 2002) which illuminates light to an inspection object (Fig. 2, Ref. 2001) containing repetitive circuit patterns formed on the surface thereof (Col. 9, lines 6-18); an optical detection

system (Fig. 2, Ref. 2006) which detects light reflected from said inspection object (Fig. 2, Ref. 2001) and transmitted through a shield unit (Fig. 2, Ref. 2004), and converts the detected light into an image signal; and a processing system which detects the defects by processing the image signal detected by said optical detection system (Col. 9, lines 44-60); wherein said shield unit (Fig. 2, Ref. 2004) is provided in said optical detection system (Fig. 2, Ref. 2006) to selectively shield diffracted light patterns (Fig. 2, Ref. 2007) coming from the repetitive circuit patterns existing on the inspection object (Fig. 2, Ref. 2001); and said shielding unit (Fig. 2, Ref. 2004) is a optically transparent substrate or substrate or a film which is etched (See Fig. 2).

**Claim 5**

Morioka et al. ('459) further discloses an optical observation unit (Fig. 2, Ref. 2003) which observers a Fourier transform image as diffraction light patterns for one chip in a Fourier transform plane, and wherein said repetitive circuit patterns comprise a plurality of chips formed on the surface of said inspection object (Col. 9, lines 6-18), and said shielding unit (Fig. 2, Ref. 2004) selectively shields the diffraction light pattern in accordance with change information of the diffraction pattern for every area in one chip in the diffraction light patterns for one chip obtained by the optical observation unit (Col. 9, lines 6-18).

**Claim 6**

Morioka et al. ('459) discloses illuminating light (Fig. 2, Ref. 2002) to an inspection object (Fig. 2, Ref. 2001) containing repetitive circuit patterns formed on a surface thereof (Col. 9, lines 6-18); detecting an image signal (Fig. 2, Ref. 2006) of transmission light by selectively shielding (Fig. 2, Ref. 2004) diffraction light pattern

(Fig. 2, Ref. 2007) generated from said repetitive circuit patterns when light is reflected from the surface of said inspection object (Fig. 2, Ref. 2001); and detecting the defects existing on the surface of the inspection object by processing the detected image signal (Col. 9, lines 6-18); wherein said repetitive circuit patterns comprise a plurality of chips formed on the surface of said inspection object (Fig. 2, Ref. 2001)(Col. 9, lines 6-18), and said selective shielding of the diffraction light pattern is performed according to a change of the diffraction light pattern for every area in one chip obtained by detecting diffraction light patterns as a Fourier transform image (Col. 9, lines 6-18).

**Claim 7**

Morioka et al. ('459) discloses an illumination optical system (Fig. 2, Ref. 2002) which illuminates light to an inspection object (Fig. 2, Ref. 2001) containing repetitive circuit patterns formed on a surface thereof (Col. 9, lines 6-18); an optical detection system (Fig. 2, Ref. 2006) which detects light reflected (Fig. 2, Ref. 2008) from said inspection object (Fig. 2, Ref. 2001) and transmitted through a shield unit (Fig. 2, Ref. 2004), and converts the detected light into an image signal; a processing system which detects the defects by processing the image signal detected by said optical detection system (Col. 9, lines 44-60); and an optical observation unit (Fig. 2, Ref. 2003) which observes a Fourier transform image as diffraction light patterns for one chip in a Fourier transform plane (Col. 9, lines 6-18); wherein said repetitive circuit patterns comprise a plurality of chips formed on the surface of said inspection object (Fig. 2, Ref. 2001) (Col. 9, lines 6-18), and said shield unit (Fig. 2, Ref. 2004) is provided in said optical detection system (Fig. 2, Ref. 2006) so as to selectively shield diffraction light patterns (Fig. 2, Ref. 2007) coming from the repetitive circuit patterns existing on the inspection object (Fig. 2,

Ref. 2001) in accordance with change information of the diffraction light pattern for every area in one chip in the diffraction light patterns for one chip obtained by the optical observation unit (Fig. 2, Ref. 2003) (Col. 9, lines 6-18).

### *Response to Arguments*

4. Applicant's arguments with respect to claims 1, 2, 4, 5 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael P. Stafira whose telephone number is 571-272-2430. The examiner can normally be reached on 4/10 Schedule Mon.-Thurs..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Toatley can be reached on 571-272-2800 ext. 77. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael P. Stafira
Primary Examiner
Art Unit 2877

March 22, 2006